	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	67	minimum adj spanning adj tree and layout and placement	USPAT; US-PGPUB	2002/11/25 12:42
2	BRS	L4	142	partitioning same layout and placement and interconnect	USPAT; US-PGPUB; DERWENT	2002/11/25 12:43

SEARCH RESULTS [PDF Full-Text (844 KB)] PREVIOUS NEXT DOWNLOAD CITATION

New algorithms for the rectilinear Steiner tree problem

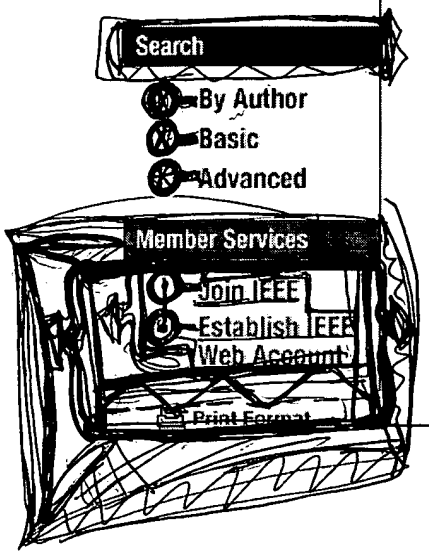
Ho, J.-M. Vijayan, G. Wong, C.K.
Inst. of Inf. Sci., Acad. Sinica, Taipei, Taiwan

This paper appears in: Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
On page(s): 185 - 193
Feb. 1990
Volume: 9 Issue: 2
ISSN: 0278-0070
References Cited: 2
CODEN: ITCSDI
INSPEC Accession Number: 3626670

Abstract:
An approach to constructing the rectilinear Steiner tree (RST) of a given set of points in the plane, starting from a minimum spanning tree (MST), is discussed. The main idea in this approach is to find layouts for the edges of the MST that maximize the overlaps between the layouts, thus minimizing the cost (i.e. wire length) of the resulting rectilinear Steiner tree. Two algorithms for constructing rectilinear Steiner trees from MSTs, which are optimal under the conditions that the layout of each edge of the MST is an L shape or any staircase, respectively, are described. The first algorithm has linear time complexity and the second algorithm has a higher polynomial time complexity. Steiner trees produced by the second algorithm have a property called stability, which allows the rerouting of any segment of the tree, while maintaining the cost of the tree, and without causing overlaps with the rest of the tree. Stability is a desirable property in VLSI global routing applications.

Index Terms:
L-shape layout; staircase layout; circuit layouts; rectilinear Steiner tree problem; minimum spanning tree; layouts; linear time complexity; polynomial time complexity; stability; VLSI global routing applications; circuit layout; computational complexity; network topology; trees (mathematics); VLSI

09/739,589



Your search matched **27** of **813209** documents.
Results are shown **25** to a page, sorted by **publication year** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the te

Then click **Search Again.**

minimum spanning tree and layout

Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **Efficient minimum spanning tree construction without Delaunay triangulation [VLSI CAD]**
Hai Zhou; Shenoy, N.; Nicholls, W.
Design Automation Conference, 2001. Proceedings of the ASP-DAC 2001. As
South Pacific , 2001
Page(s): 192 -197

[Abstract] [PDF Full-Text (468 KB)] **CNF**

2 **Optimal layout of hexagonal minimum spanning trees in linear tim**
Lin, G.-H.; Xue, G.
Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEI
International Symposium on , Volume: 4 , 2000
Page(s): 633 -636 vol.4

[Abstract] [PDF Full-Text (356 KB)] **CNF**

3 **Computing hexagonal Steiner trees using PCx [for VLSI]**
Thurber, A.P.; Guoliang Xue
Electronics, Circuits and Systems, 1999. Proceedings of ICECS '99. The 6th I
International Conference on , Volume: 1 , 1999
Page(s): 381 -384 vol.1

[Abstract] [PDF Full-Text (224 KB)] **CNF**

4 **Approximating hexagonal Steiner minimal trees by fast optimal lay minimum spanning trees**
Guo-Hui Lin; Guoliang Xue; Defang Zhou

Computer Design, 1999. (ICCD '99) International Conference on , 1999
Page(s): 392 -398

[Abstract] [PDF Full-Text (124 KB)] **CNF**

---

5 **Finding obstacle-avoiding shortest paths using implicit connection**
Zheng, S.Q.; Joon Shink Lim; Iyengar, S.S.
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactio
Volume: 15 Issue: 1 , Jan. 1996
Page(s): 103 -110

[Abstract] [PDF Full-Text (968 KB)] **JNL**

---

6 **Simultaneous routing and buffer insertion for high performance interconnect**
Lillis, J.; Chung-Kuan Cheng; Ting-Ting Y. Lin
VLSI, 1996. Proceedings., Sixth Great Lakes Symposium on , 1996
Page(s): 148 -153

[Abstract] [PDF Full-Text (520 KB)] **CNF**

---

7 **Routing using implicit connection graphs [VLSI design]**
Zheng, S.Q.; Lim, J.S.; Iyengar, S.S.
VLSI Design, 1996. Proceedings., Ninth International Conference on , 1995
Page(s): 49 -52

[Abstract] [PDF Full-Text (396 KB)] **CNF**

---

8 **Prim-Dijkstra tradeoffs for improved performance-driven routing t design**
Alpert, C.J.; Hu, T.C.; Huang, J.H.; Kahng, A.B.; Karger, D.
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactio
Volume: 14 Issue: 7 , July 1995
Page(s): 890 -896

[Abstract] [PDF Full-Text (644 KB)] **JNL**

---

9 **A buffer distribution algorithm for high-performance clock net opti**
Jun-Dong Cho; Sarrafzadeh, M.
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume 1 , March 1995
Page(s): 84 -98

[Abstract] [PDF Full-Text (1304 KB)] **JNL**

10 **On Steiner tree problem with 45/spl deg/ routing**
Lee, D.T.; Shen, C.-F.; Ding, C.-L.
Circuits and Systems, 1995. ISCAS '95., 1995 IEEE International Symposiun
Volume: 3 , 1995
Page(s): 1680 -1682 vol.3

[Abstract] [PDF Full-Text (228 KB)] **CNF**

11 **An edge-based heuristic for Steiner routing**
Borah, M.; Owens, R.M.; Irwin, M.J.
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactio
Volume: 13 Issue: 12 , Dec. 1994
Page(s): 1563 -1568

[Abstract] [PDF Full-Text (480 KB)] **JNL**

12 **Closing the gap: near-optimal Steiner trees in polynomial time**
Griffith, J.; Robins, G.; Salowe, J.S.; Tongtong Zhang
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactio
Volume: 13 Issue: 11 , Nov. 1994
Page(s): 1351 -1365

[Abstract] [PDF Full-Text (1340 KB)] **JNL**

13 **Rectilinear Steiner tree construction by local and global refinemer**
Ting-Hai Chao; Yu-Chin Hsu
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactio
Volume: 13 Issue: 3 , March 1994
Page(s): 303 -309

[Abstract] [PDF Full-Text (668 KB)] **JNL**

14 **A direct combination of the Prim and Dijkstra constructions for im performance-driven global routing**
Alpert, C.J.; Hu, T.C.; Huang, J.H.; Kahng, A.B.
Circuits and Systems, 1993., ISCAS '93, 1993 IEEE International Symposiun 1993
Page(s): 1869 -1872 vol.3

[Abstract] [PDF Full-Text (380 KB)] **CNF**

15 **m3D: A multidimensional dynamic configurable router**
Wiley, C.; Lau, K.M.; Szygenda, S.A.
Circuits and Systems, 1993., ISCAS '93, 1993 IEEE International Symposiun 1993
Page(s): 1857 -1860 vol.3

[Abstract] [PDF Full-Text (464 KB)] **CNF**

16 **Efficient maze-running and line-search algorithms for VLSI layout**
Zheng, S.-Q.; Lim, J.S.; Iyengar, S.S.
Southeastcon '93, Proceedings., IEEE , 1993
Page(s): 7 p.

[Abstract] [PDF Full-Text (596 KB)] **CNF**

17 **On the performance bounds for a class of rectilinear Steiner tree h in arbitrary dimension**
Kahng, A.B.; Robins, G.
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactio
Volume: 11 Issue: 11 , Nov. 1992
Page(s): 1462 -1465

[Abstract] [PDF Full-Text (312 KB)] **JNL**

18 **Provably good performance-driven global routing**
Cong, J.; Kahng, A.B.; Robins, G.; Sarrafzadeh, M.; Wong, C.K.
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactio
Volume: 11 Issue: 6 , June 1992
Page(s): 739 -752

[Abstract] [PDF Full-Text (1172 KB)] **JNL**

19 **A wire-length minimization algorithm for single-layer layouts**
Chen, D.-S.; Sarrafzadeh, M.
Computer-Aided Design, 1992. ICCAD-92. Digest of Technical Papers., 1992 International Conference on , 1992
Page(s): 390 -393

[Abstract] [PDF Full-Text (332 KB)] **CNF**

20 **Fast vicinity-upgrade algorithm for rectilinear Steiner trees**
Chua, J.K.; Lim, Y.C.
Electronics Letters , Volume: 27 Issue: 13 , 20 June 1991
Page(s): 1139 -1141

[Abstract] [PDF Full-Text (248 KB)] **JNL**

---

21 **A Steiner tree construction for VLSI routing**
Kahng, A.B.
Neural Networks, 1991., IJCNN-91-Seattle International Joint Conference on i , 1991
Page(s): 133 -139 vol.1

[Abstract] [PDF Full-Text (408 KB)] **CNF**

---

22 **On clock routing for general cell layouts**
Cong, J.; Kahng, A.; Robins, G.
ASIC Conference and Exhibit, 1991. Proceedings., Fourth Annual IEEE Interr 1991
Page(s): P14 -5/1-4

[Abstract] [PDF Full-Text (352 KB)] **CNF**

---

23 **New algorithms for the rectilinear Steiner tree problem**
Ho, J.-M.; Vijayan, G.; Wong, C.K.
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactio Volume: 9 Issue: 2 , Feb. 1990
Page(s): 185 -193

[Abstract] [PDF Full-Text (844 KB)] **JNL**

---

24 **Rectilinear Steiner tree construction by local and global refinemer**
Chao Ting-Hai; Hsu Yu Chin
Computer-Aided Design, 1990. ICCAD-90. Digest of Technical Papers., 1990 International Conference on , 1990
Page(s): 432 -435

[Abstract] [PDF Full-Text (364 KB)] **CNF**

---

25 **A new class of Steiner tree heuristics with good performance: the 1-Steiner approach**
Kahng, A.; Robins, G.
Computer-Aided Design, 1990. ICCAD-90. Digest of Technical Papers., 1990 International Conference on , 1990
Page(s): 428 -431

[Abstract] [PDF Full-Text (308 KB)] **CNF**

1 2 [Next]

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search
Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting
No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ | Terms | Back to Top